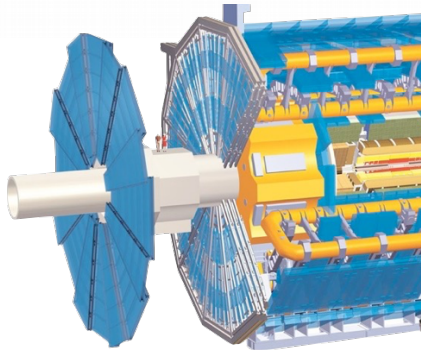
TEXAS
The University of Texas at Austin

ATLAS EXPERIMENT



Comparator Design Optimization

Ray Xu

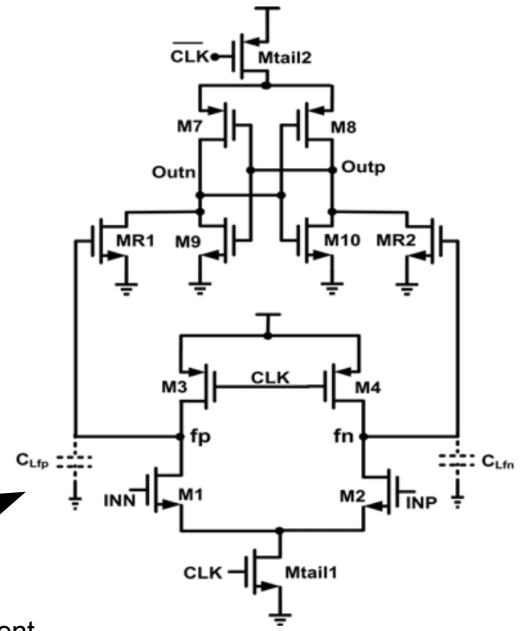
Jan 27, 2017

Three Designs

- Three Designs
  - Double-tail Comparator 1 (“DTC1”)
  - Single-phase DTC (Chen-Kai’s design)
  - Double-regenerative DTC (“DTC2”) (new design)
- Transistor-level Optimization
- Testbench
- Performance Comparison
- Summary of Design Tradeoffs

Double Tail Comp. 1

- The “original” double-tail design
- CLK=0 → Pre-charge capacitance on nodes fn and fp to VDD
- CLK=1 → fn and fp discharge
- During discharge: $|V_{fp} - V_{fn}|(t) \propto \frac{\Delta V_{IN} \times g_{m1,2} \times t}{C_{fp,n}}$
- Input with the lesser voltage discharges first → its respective output goes to zero on the second-stage x-inverter.



Symbolic capacitor; not a lumped component...

Figure from [1]

Single-Phase DTC

- Structurally similar to DTC1; same theory of operation
- $\overline{\mathrm{CLK}}$ is replaced with one additional PMOS & NMOS
- The additional NMOS & PMOS equate to an effective gm boost of 2x ~ 3x in the second stage

  → 2x ~ 3x faster response time

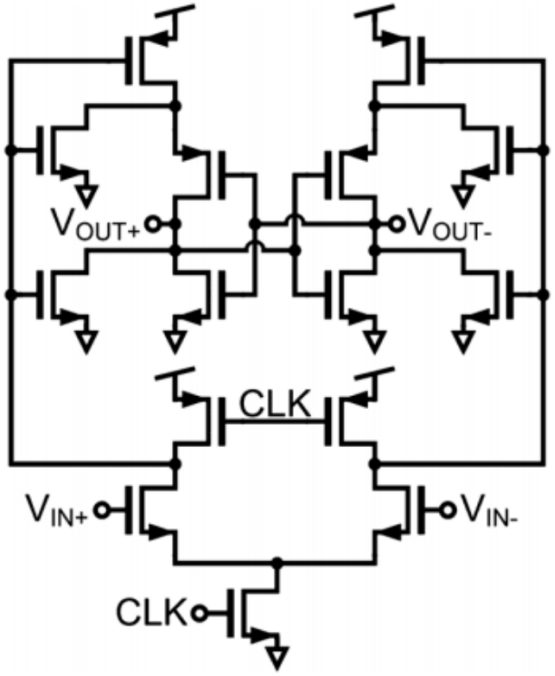


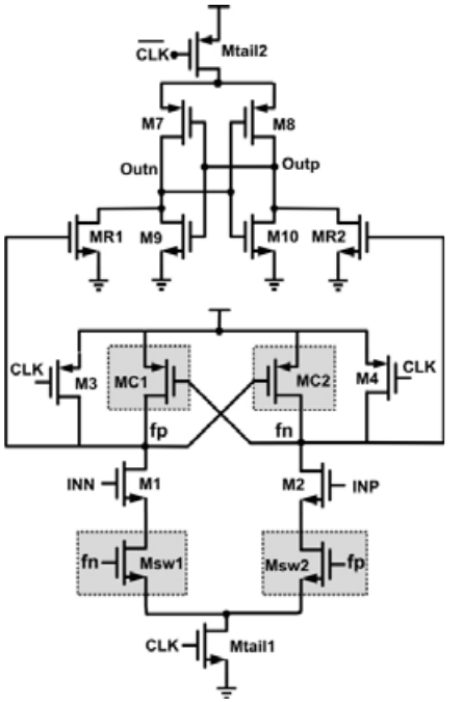
Figure from [2]

Double-Regenerative DTC

- Design proposed in [1]
- First stage is replaced with a regenerative stage
- Unlike the original DTC, V_{fn} and V_{fp} discharge rate is **exponential**

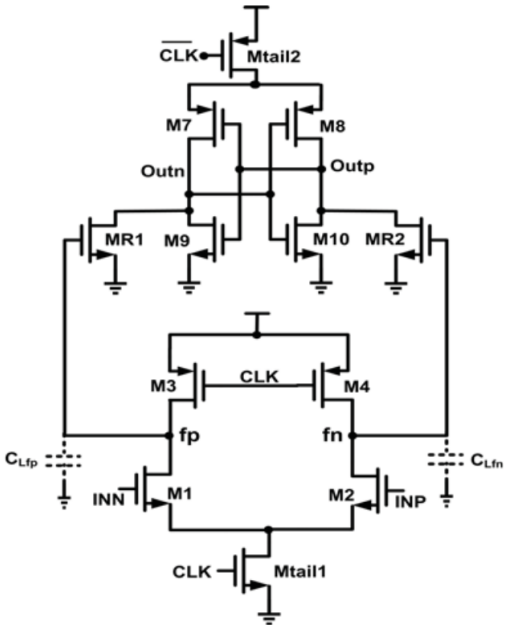
$$\{|V_{fp}-V_{fn}|\}(t) \propto \Delta V_{IN} \exp\left(\frac{g_{m1,2} \times t}{C_{fp,n}}\right)$$

- M_{sw1} & M_{sw2} used to avoid static DC flow



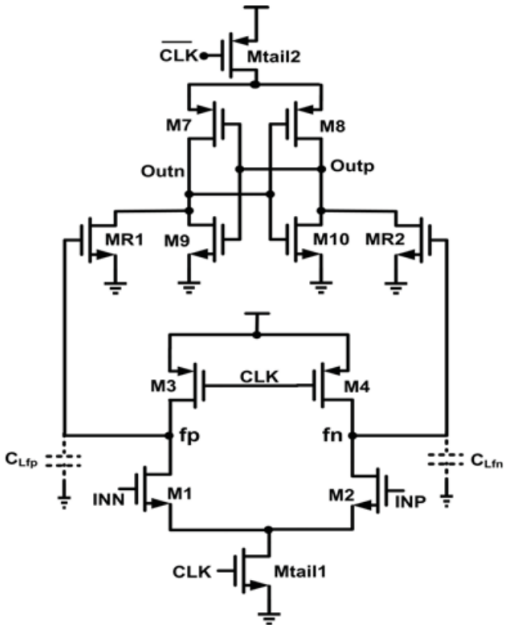
DTC1 Guidelines

- First stage:
  - Larger $\mathrm{M1}, \mathrm{M2} \rightarrow$ faster decision time but more power
  - If discharge rate is too high → risk of false latching (high noise); inadequate $\{|V_{\mathrm{fp}} - V_{\mathrm{fn}}|\}$
- Large $\mathrm{M}_{\mathrm{tail1}}, \mathrm{M}_{\mathrm{tail2}} \rightarrow$ low $\mathrm{V}_{\mathrm{DS,ON}}$
- Don't use min length for analog transistors (L = 130 nm)
- Even number of fingers & multiplier for easier matching in layout (pref. m=8)



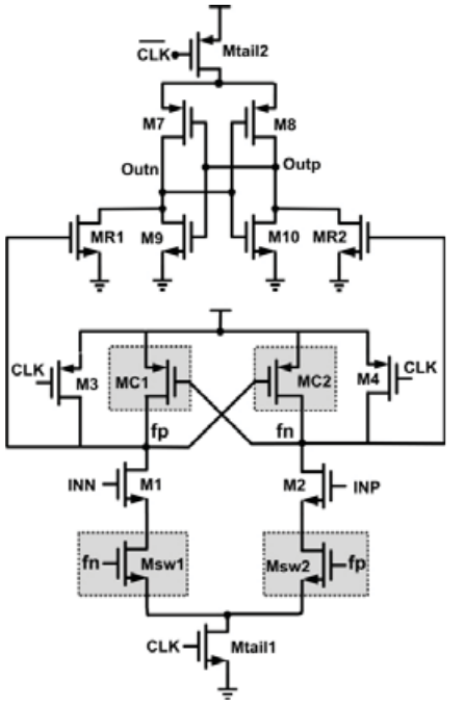
DTC1 Guidelines (cont.)

- Second stage:
  - Min size inverters → low cross-over power consumption
  - $g_{mR1} > g_{m9}$ and $g_{mR2} > g_{m10}$ for stronger sensitivity to positive feedback, but slower response time
  - Large $C_{fp,n}$ → less noise; less false latching, but slower response time (higher time const., lower kT/C noise)
- Buffer on $Outn$ and $Outp$ to prevent perturbing the positive feedback on the min-size inverters



Double-Regen. Guidelines

- First stage:
  - Regeneration in 1st stage → allows larger M1 & M2 (for less false-latching, faster response time, etc) without as much of a power penalty
  - Weaker $\mathrm{MC1}$ & $\mathrm{MC2}$, but stronger $\mathrm{Msw1}$ & $\mathrm{Msw2}$ → keeps power low
- Second stage:
  - g_{mR1} and g_{mR2} need not to be as large due to exponential growth
  - $\mathrm{MR1}$ & $\mathrm{MR2}$ now mostly determined by max. false-latching (noise) spec.
  - Move most of $C_{fp,n}$ to $\mathrm{M3}$ and $\mathrm{M4}$
  - Faster response time



Testbench

- CLK: 320 MHz, 1000 cycles
- V_{IN+} = 600.0mV; V_{IN-} = 600.4 mV (recall 1LSB ≈ 977 uV)
- Two min-sized inverters (buffer) placed on each output
- 5 fF load on each output
- Transient sim, conservative accuracy, trans. Noise
  - Fmin = 1 Hz, Fmax = 100 GHz, Seed = 1, Scale = 1
- Input-referred noise spec [3]:

$$P[\text{Incorrect}] = erfc\left(\frac{\Delta V_{IN}}{\sigma\sqrt{2}}\right)$$

Performance Comparison

	DTC1	Single-phase DTC (Chen-Kai's design)	Double-Regen (DTC2)
Avg. Power @ 320 MHz	103.5 μW	78.83 μW	102.3 μW
Prop. Delay $t_{CLK \rightarrow OUT}$	210 pS	130 pS	127 pS
P[correct] n=1000	96.6 %	91.9 %	96.5 %
			97.2 % @ 120 μW
Input-referred σ ("input-ref. noise")	189 μV	229 μV	190 μV
ΣC_{fn}	98.178 fF	24.07 fF	69.37 fF
Input transistor gate area (pre-layout), per transistor	1.04 μm^2 L = 130 nm	2.88 μm^2 L = 60 nm	4.16 μm^2 L = 130 nm

Summary

- DTC1 has too many trade-offs relying on a few transistors
- Adding regenerative first stage allows for more flexibility
  - More transistors to play around with…
  - Exponential growth, as opposed to linear, in first stage eases second stage requirements
- Can be optimized even further for a single parameter instead of overall performance…

To-do

- Monte Carlo/corner simulations
- Further optimization?
- Optimization of other ADC components?
- Design of reference buffer
- Start layout (w/ Chen-Kai)
- Things to think about:
  - Layout: use of waffle/annular ring transistors for rad-hardness?
  - Fail-safe/redundancy circuitry to mitigate SEE/SEU's?
  - Additional circuits to fit into tapeout to study SEE/SEU? (probably not ADC related)

Reference

1. S. B. Mashhadi and R. Lotfi, “Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator,” ***IEEE Trans. On VLSI***, Vol. 22, No. 2, February 2014
2. Y. Lim and M.P. Flynn, “A 1mW 71.5dB SNDR 50 MS/S 13b fully differential ring-amplifier-based SAR-assisted pipeline ADC,” in ***Proc. IEEE ISSCC. Dig. Tech. Papers***, Feb. 2015, pp. 1–3.
3. https://everynanocounts.com/2013/06/25/noise-effect-on-the-probability-of-comparator-decision/